Influence of deposition temperature and front gate materials on negative fixed charges at alumina-silicon interfaces
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Influence of deposition temperature and front gate materials on negative fixed charges at alumina-silicon interfaces

By

Yuxing Cui

A Thesis

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Influence of deposition temperature and front gate materials on negative fixed charges at alumina-silicon interfaces

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Abstract

In this paper, the negative fixed charge at alumina-silicon interfaces is investigated. First, sample electrical behavior after aging in a glove box for eight months was investigated and the capacitance-voltage (C-V) curves did not significantly change. It means the negative fixed charges are very stable at alumina-silicon interfaces. Additionally, the relationship between negative fixed charges and the deposition temperature is discussed. The negative fixed charges increase when deposition temperature decreases. In my work, samples deposited at 150 °C have the highest negative fixed charges in the film – almost -1.8×10^{12}q/cm^2. Finally, MOSCaps have been fabricated with different front gates, like Al, Ni. Only samples with Al front gate have negative fixed charges. For nickel samples, the results are just the opposite(+4.70×10^{11}q/cm^2 and +3.93×10^{11}q/cm^2).
1 Introduction

1.1 Semiconductor Dielectric Interface

1.1.1 Metal-Oxide-Semiconductor-Field Effect Transistor (MOSFET)

The Metal-Oxide-Semiconductor-Field Effect Transistor (MOSFET) is widely used in analog circuits and digital circuits since 1959. Figure 1 shows the structure of PMOSFET, which consisted of three electrodes (Source, Gate, Drain) insulating layer and a body.

![Figure 1. Structure of PMOSFET](image)

Because of Moore’s law, the size of the transistors has become smaller and smaller in recent years to satisfy the requirements of new generation semiconductor devices. Thus, the gate oxide becomes thinner and thinner. However, when the thickness of the gate oxide...
reached to 1.2nm (5 atoms thick), the tunneling effect causes more leakage current \[^1\]. Figure 2 shows this situation \[^2\].

The drive current can be calculated by Eq. 1\[^3\]. By using this equation, gate oxide should have high capacitance. In the other word, when the thickness of gate oxide is very thin, new materials of gate oxide should have a high dielectric constant.

\[
I_{D,sat} = \frac{W}{2L} \mu C_{ox} (V_G - V_{TH})^2 \quad \text{where} \quad C_{ox} = \frac{k\varepsilon_0 A}{t_{ox}}
\]

In Eq. 1, \( k \) is the dielectric constant, \( t_{ox} \) is the thickness of gate oxide, \( A \) is contact area, \( \varepsilon_0 \) is the permittivity.

Besides, dielectric layers need to be smooth to prevent the phonons scatter electrons in the channel \[^3\]. All these problems mentioned can be solved by High-k materials synthesized by ALD (Atomic Layer Deposition), like ALD Al\(_2\)O\(_3\).

### 1.1.2 Solar cells

The Solar cell is a device that can convert the solar energy into electricity. To improve the efficiency of the solar cell, the surface recombination velocities should be very low. Passivating the silicon surface can achieve this goal. There are two strategies to passivate
the surface of silicon to solve this problem. The first strategy is called chemical passivation. At the silicon surface, many defect states exist, which will recombine with electrons and holes to increase the recombination rate. Thus, reducing the interface defect can be the method to passivate the surface of silicon. The second strategy is called field-effect passivation. This strategy can be achieved by the reduction of minority carrier concentration. The combination is decided by both electrons and holes, so when the amount of one of them is very small, the recombination rate will decrease $^{[4,8]}$. ALD technology could help to passivate the surface of silicon.

1.2 Atomic Layer Deposition and ALD Al$_2$O$_3$

1.2.1 Fundamental of Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a powerful thin film growth technique. Compared with other deposition methods, such as thermal vapor deposition, this thin film growth technique can accurately control the thickness of the layer in the nanometer level. This advantage helps ALD attract more attention from the IC industry thanks to the growing requirements for the size of semiconductors in recent years $^{[5]}$. Besides, due to the gaseous precursors during the reaction, this method can deposit thin films on any geometry of surfaces $^{[6]}$. But ALD’s deposition rate is very slow because of the accuracy control. This is one of the main disadvantages of using the ALD to control the deposition thickness accuracy $^{[7]}$. 
Figure 3 shows a general procedure of using the ALD method [7]. During one cycle ALD, precursor A is pumped into the reaction chamber and reacts with the functionalized surface of substrate. Then, inert gases have been injected to purge excess precursor A and some useless reaction products. After that, precursor B is pumped into the reaction chamber and reacts with the surface which is consisted of precursor A. Then, inert gases have been injected to purge excess precursor B and some useless reaction products. Thus, a single-layer desired material thin film has been deposited on the substrate. Repeating the same procedure until the thickness of the desired material has been reached. The thickness of each single-layer is almost the same and can be confirmed. Thus, by controlling the cycle numbers of ALD, the thickness of layer can be accurately determined at the nanometer level.
1.2.2 ALD Al₂O₃

Al₂O₃ is an effective material for surface passivation of crystalline silicon (c-Si) based solar cells. There are many methods used to deposit Al₂O₃, like sputtering and plasma-enhanced chemical vapor deposition (PECVD). Compared to these deposition techniques, the growth rate is lower by using ALD technology. However, ALD Al₂O₃ has a better surface passivation quality [8].

ALD Al₂O₃ has low level of interface trap density (~ 10¹¹ eV⁻¹cm⁻²) [1]. Thus, ALD Al₂O₃ lower the interface defects trap density between the Al₂O₃/Si surface to achieve the chemical passivation. Meanwhile, ALD Al₂O₃ has a higher negative fixed charge which can suppress electron concentration near the Al₂O₃/Si surface to achieve field-effect passivation.

For solar cells, ALD Al₂O₃’s bandgap is more than 6.2 eV, which is also the advantage of using the ALD method [9]. Because the energy of solar radiation is almost in the visible and infrared part (wavelength > 400 nm), the bandgap of materials of passivation film should larger than 3.1 eV to avoid absorbing the visible and infrared part of the solar spectrum [10].

1.3 Fixed charges of ALD Al₂O₃

Just like the previous section mentioned, ALD Al₂O₃ have a higher negative fixed charge density. There is a theory to explain the origin of these negative fixed charges. The negative fixed charge (Qf) comes from O dangling bonds (O DBs) which are formed by Al vacancies, O interstitials [4]. Kimoto et al. found tetrahedral- and octahedral-coordinated Al
atoms contained in the ALD Al₂O₃. Most tetrahedral coordination accumulates close to the interface \[^{[11]}\]. For Lucovsky, the ratio of amorphous Al₂O in its local molecular structure between tetrahedral-coordinated Al in AlO\(_{4/2}^-\) and octahedral-coordinated Al\(^{3+}\) is 3:1 to meet the requirement of charge neutrality \[^{[12]}\]. Because the tetrahedral AlO\(_{4/2}^-\) dominates near the surface of Al₂O₃, it causes the formation of an O-rich condition which contributes to O interstitials. In other words, because of the domination of tetrahedral AlO\(_{4/2}^-\), lacking octahedral Al\(^{3+}\). This situation makes the existence of Al vacancies near the surface \[^{[13]}\]. B.Hoex et al. demonstrated H interstitials also contributes negative fixed charges. During the Al₂O₃ composed by ALD, precursors Trimethyl Aluminum (TMA) and H₂O contain H and H interstitials may be formed \[^{[14]}\].

### 1.4 Hypothesis

There are several hypotheses in this paper. First, the previous section mentions that the negative fixed comes from O dangling bonds \[^{[4]}\]. The structure of Al₂O₃ will be difficult to change in the normal environment. If samples are stored in the glove box for a long time, the negative fixed charges should be very stable at alumina-silicon interfaces. Second, Sung-Kwen Oh’s \[^{[4]}\] experiments show, above 250°C, negative fixed charges are decreased with deposition temperature increasing. At lower deposition temperature, if deposition temperature decreases, the negative fixed charges will be increased.
2 Experiment

2.1 Sample preparation

2.1.1 Wafer clean

Before the ALD, the metallic and organic contamination had been removed in the cleaning process for the wafer. In some cases, the native oxide had been removed by using Hydrofluoric Acid (HF). The wafer cleaning procedure included three parts in this experiment, cutting, sonicating in the isopropanol (IPA), and the standard Radio Corporation of America clean (RCA-1+RCA-2), HF.

The functionalized substrate used in this experiment is the single-side polished n-type silicon wafer whose orientation is <1 0 0>. It can be cleaved by a diamond-tipped scribe and a ruler to the 1” × 1” silicon wafers. After that, silicon wafers were submerged into IPA contained in the test tubes. Test tubes were placed into a sonicator bath for 5 mins. The bath surface should over the IPA surface in test tubes. IPA was poured out from test tubes and these wafers were rinsed with deionized water (18.2 MΩ). Finally, silicon wafers were transferred into the Teflon rack for RCA cleaning.

For RCA cleaning procedure, which includes RCA-1, RCA-2 step. In this procedure, the first step was submerging the silicon wafers in the RCA-1 solution (NH₄OH-H₂O₂-H₂O 1:1:5) at 70-80 °C for 10 mins to remove organic contaminants, then rinsing wafers with deionized water. The second step was submerging the silicon wafers in RCA-2 solution
(HCl-H₂O₂-H₂O 1:1:6) at 70-80 °C for 10 mins to remove metallic contaminants, then wafers were rinsed with deionized water. All the water used to make the above solutions were deionized water.

For several cases, the native oxide was needed to be removed. The wafers were etched by submerging them into 5% HF for 30 seconds, then they were rinsed two times by using deionized water. After that, the surface of wafers became hydrophobic.

In the final step for the wafer cleaning process, a nitrogen gun was used to dry the silicon wafers and dried silicon wafers were placed into the plastic containers which have been labeled to best describe wafers.

2.1.2 Oxide film deposition (ALD)

In this experiment, all thin films were deposited by using atomic layer deposition (ALD). Figure 5 shows the “Savannah” ALD system which was used in this experiment. The precursors used to make ALD Al₂O₃ films were Trimethyl Aluminum (TMA) and H₂O

![Figure 4. “Savannah” ALD system](image)
in this experiment. Table 1 shows the ALD recipe obtained at 150 °C. For low deposition temperatures, water is liquid. Thus, purge time (Table 2) is more than the normal purge time to remove the H₂O and precursors completely [15]. The growth rate was almost 0.9 Å/cycle at 150°C.

<table>
<thead>
<tr>
<th>Precursor</th>
<th>Pulse time (sec)</th>
<th>Purge time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMA</td>
<td>0.025</td>
<td>8</td>
</tr>
<tr>
<td>H₂O</td>
<td>0.08</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 1. ALD recipe at 150°C

<table>
<thead>
<tr>
<th>Deposition temperature (°C)</th>
<th>TMA purge time (sec)</th>
<th>H₂O purge time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td>80</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>100</td>
<td>15</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 2. ALD recipe from 50°C to 100°C

2.1.3 Annealing procedure

The annealing procedure was a good way to remove the trap density [16] and make thin-film dense [17]. In this experiment, all the samples were annealed in N₂ atmosphere. Quartz Boat was used to hold samples. For most of these experiments, ramp time was 60 min, the annealing temperature used was 425°C or 450°C, and dwell time was 20 min.
2.1.4 Front gate and back contact deposition

The thermal evaporation (Figure 6) technique was used to deposit aluminum front gates in this experiment. A quartz-crystal microbalance (QCM) was used to detect the thickness of metal and pasted the Molybdenum shadow mask (Figure 7). For back contact, InGa and Ag pasted by Aluminum plate were used as back contact.

Figure 5. Denton Thermal Evaporation

Figure 6. Shadow mask
2.2 Film Characterization

2.2.1 Spectroscopic Ellipsometry (SE)

In this experiment, spectroscopic ellipsometry (J.A Woolam Vase system) was used to get the thickness of the Al$_2$O$_3$ film. The incident beam’s angle was from 60° to 70° and the step was 10°. The wavelength used was from 350 nm to 800 nm and the step was 15 nm. The data were fitted by Cauchy equation: $n(\lambda) = A + B/\lambda^2 + C/\lambda^4$, where $n$ is the refractive index, $\lambda$ is the wavelength, $A$, $B$, $C$ is the coefficients determined by the properties of materials. Native oxide thickness was assumed as 15 Å.

2.2.2 Optical Microscope

For this experiment, an optical microscope was used to measure the gate size and observe the morphology of the surface. Through the optical microscope, the quality of Al$_2$O$_3$ thin film was confirmed by observing the existence of blisters. Meanwhile, the gate surface’s damage status caused by probe contact during electrical measurements and the area which was used to calculate the $N_f$ were checked. This was a factor that can affect final results when doing the C-V measurements.

2.3 Electrical measurements

2.3.1 MOS capacitors

In this work, the quantities of negative fixed charges at the alumina-silicon interface were measured by testing Metal-Oxide-Semiconductor capacitors (MOSCaps). The
MOSCaps is made of the front gate (metal), an oxide film (insulator), the semiconductor substrate and back contact. To achieve the function of capacitors, the thickness of the oxide film was over 1.2 nm in order to prevent the current leakage \[^1\]. In these experiments, InGa and silver acted as back contacts. Compared with the traditional back contact—aluminum, these back contacts can save much more time and save huge costs. Ag only needs to be applied and scratch the back of the semiconductor to create the good ohmic contact. Figure 8 shows the MOSCaps’ structure with different back contact.

2.3.2 Capacitance – Voltage Measurement

The Capacitance-Voltage(C-V) measurement is a good way to measure the electrical properties of semiconductors and related devices. According to Eq. 2 \[^{18}\], we can get the capacitance of MOSCaps, which is

\[
C = \frac{C_{ox}(C_p+C_b+C_n+C_{it})}{C_{ox}+C_p+C_b+C_n+C_{it}}
\]  \hspace{1cm} (2)
C\textsubscript{ox} is oxide layer capacitance, C\textsubscript{p} is hole charge capacitance, C\textsubscript{b} is space charge capacitance, C\textsubscript{n} is electron charge capacitance, C\textsubscript{it} is interface states capacitance. Thus, MOSCaps’ capacitance likes \(C\textsubscript{p}, C\textsubscript{b}, C\textsubscript{it}\) and \(C\textsubscript{n}\) were connected in parallel, then in series with \(C\textsubscript{ox}\) (figure 8) \[18\]. During these experiments, all MOSCaps were n-type. Figure 9 shows the n-type C-V curve at very high frequency (100000Hz) ac voltage.

![Figure 8. C-V curve (n-type MOSCap)](image)

![Figure 9. Equivalent capacitance circuit](image)

For n-type substrate, when gate voltages are more than \(V\textsubscript{fb}\), electrons heavily accumulate on the oxide and semiconductor surface. Only \(C\textsubscript{n}\) works and \(C\textsubscript{n}\) is almost a short circuit. Thus, the total capacitance is \(C\textsubscript{ox}\). When gate voltages gradually are reduced and less than \(V\textsubscript{fb}\), the surface becomes depletion (surface’s electrons and holes are recombined). The interface trapped charges and space charges dominate. The equivalent capacitance is \(C\textsubscript{ox}\) in series with \(C\textsubscript{b}\) and \(C\textsubscript{it}\) are connected in parallel. At negative voltage, the inversion region begins appearing and hole charges gradually dominate. When inversion charges (hole charges for n-type) could follow the ac voltage, just like the accumulation region, only \(C\textsubscript{p}\) works and total capacitance is \(C\textsubscript{ox}\). However, inversion
charges could not follow the ac voltage at very high frequency. The total capacitance is $C_{ox}$ in series with $C_b^{[18]}$.

In this experiment, the HP4194A gain-phase analyzer (figure 11) was used to do the C-V measurements with a Signatone probe. All the C-V curves came from C-V measurement applied 100000 Hz ac voltage in these experiments.

![Figure 10. HP4194A gain-phase analyzer](image)
3 Results and Discussion

In this experiment, samples were placed in the dark, metal box which could be prevented electrical-field and charges caused by illumination and measured by HP4194A. The data got by the analyzer could be transferred into the C-V curves by using MatLab. Figure 12 shows the C-V results related to two different measuring times. Some C-V curves of pads in the sample deposited at 150 ℃ shifted just a little in an accumulation region which means oxide layer capacitance change a little and most curves perfectly coincided after 8 months remeasurement. For the 250 ℃ sample, each curve coincided in an accumulation region. Only one pad’s curve shifted a little to the left, the rest of red curves (8 months ago) almost cover the black line. These little changes indicated the negative
fixed charges in this pad changed a little \cite{19} or a human error created during the measurement procedure. These factors do not influence on the final result. According to most data obtained during the experiment, the conclusion is that the negative fixed charges are very stable at alumina-silicon interfaces.

Figure 13 shows the comparable C-V curves at three different deposition temperatures. These curves were obtained by measuring the nine pads in each sample from negative to positive voltages. Compared with the 250 °C sample (red line), total curves (green line) of the sample deposited at 200 °C shifted to right a little and area normalized capacitance was elevated much in an accumulation region, which indicated that there had more negative fixed charges in the 200 °C sample \cite{20}. Although area normalized

![Figure 13. Comparable C-V about three different deposition temperature: 150°C, 200°C and 250°C](image-url)
capacitance of 150 and 250 °C samples are almost the same in the accumulation region, 150 °C sample curves shifted a very large step to right compared to that at 250 degrees. It meant the negative fixed charges increased more. Compared with the 200 °C sample, C-V curves were lower in the accumulation region but shifted lots to the right in the 150 °C sample, which meant the 150 °C sample had more negative fixed charges.

Table 3. The fixed charge density at three different deposition temperature

<table>
<thead>
<tr>
<th>Deposition temperature (°C)</th>
<th>Average-N_f(q/cm^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>-1.8E+12</td>
</tr>
<tr>
<td>200</td>
<td>-1.3E+12</td>
</tr>
<tr>
<td>250</td>
<td>-0.796E+12</td>
</tr>
</tbody>
</table>

Figure 13 and Table 3 directly quantify the negative fixed charge density in MOSCaps.

The negative fixed charge is calculated by Eq. 3 \[^{20}\]
\[ N_f = \frac{C_{ox}(\phi_{MS} - qV_{fb})}{qA} \]  

Where \( C_{ox} \) is oxide capacitance, \( V_{fb} \) is the flat-band voltage. These values can be obtained by C-V measurements. \( \phi_{MS} \) is the work function difference between metal and semiconductor. \( A \) is the area of the circle pad. The sample deposited at 150 °C had higher negative fixed charges in the film – almost \(-1.8 \times 10^{12} \text{q/cm}^2\). The trend showed the negative fixed charges increased with deposition temperature decreasing above 150 °C. Because the negative fixed charges contribution comes from O interstitials, H interstitials and Al vacancies \[^4,14\]. With deposition temperature decreasing, Al/O ratio has been decreased in the Al\(_2\)O\(_3\) thin film \[^21,23\]. It creates the O-rich situation at the interface which will contribute to O interstitials. Meanwhile, the amount of hydrogen is increased when the deposition temperature decrease \[^22,23\]. Thus, there has a very high probability to make H interstitials at low deposition temperature. All these cause the trend displayed in figure 14 -- the negative fixed charges increase with deposition temperature decreasing.

This part, the goal of this experiment is to investigate the influence of different front gates (Al & Ni) on negative fixed charges of MOSCaps. The C-V curves (figure 15a) almost coincided which means 9 pads in the sample with Al.
front gate was consistent. The $C_{ox}$ range was from $2.169 \times 10^{-9}$ to $2.271 \times 10^{-9}$ F, $V_{fb}$ range was from 0.78-0.92 V. For nickel front gate, some curves separated from each other in two samples. Thus, the pads were not consistent. One sample’s (15b) $C_{ox}$ range was from $2.296 \times 10^{-9}$ to $2.582 \times 10^{-9}$ F, $V_{fb}$ range was from 0.48-0.78 V. For another sample(15c), $C_{ox}$ range was from $2.442 \times 10^{-9}$ to $2.855 \times 10^{-9}$ F, $V_{fb}$ range was from 0.47-0.86 V.

Figure 14. C-V curves of different front gate MOSCaps (a) Al (b) Ni 1 (c) Ni 2
Figure 16 displayed the density of fixed charge. Only the aluminum front gate had negative fixed charges (-2.57×10^{12}q/cm^2) and a very small error bar. The density of the fixed charge of nickel front gate samples was +4.70×10^{11}q/cm^2 and +3.93×10^{11}q/cm^2, respectively.

Figure 15. The density of fixed charge of Al, Ni front gate MOSCaps
4 Conclusions

The negative fixed charges are almost the same and stable at silicon-aluminum interfaces in the normal environment, where the structure of Al₂O₃ is difficult to be changed.

Above 150 °C, the negative fixed charges are increased by decreasing the deposition temperature. The environment is more likely O-rich and H-rich at the surface of ALD Al₂O₃ created at lower deposition temperature, which will have a high probability to create more O and H interstitials that contribute to native fixed charges.

In this paper, only the sample with Al front gate has negative fixed charges. For MOSCaps which want to have a larger negative fixed charge in the film, nickel is not a suitable material to make the front gate.
Reference


Yuxing Cui was born on September 11th, 1993 to Zhenghong Cui and Haiping Du. After finishing his bachelor’s degree in Renewable Energy Materials and Devices in the University of Electronic Science and Technology of China, he received admission from Binghamton University for a Master’s program in Materials Science and Engineering. After 4-month learning in Binghamton university, he transferred to Lehigh University and followed Professor Nicholas in the department of Materials Science and Engineering. In the beginning, he learned some technologies and worked with Ideal Semi company. Under his advisors’ guidance, he had a chance to finish his master’s thesis. After graduation, he plans to work in China in the related company, trying to apply skills he learned to his work. Maybe, in the future, he will pursue a Ph.D. to make a more thorough research on his professional field.